IC-INT-VPX3c

Intel® Core™ i7 (Gen3) SBC

The **IC-INT-VPX3c** is based on the Intel® Core™ i7 processor Ivy Bridge and its companion chipset QM77. This generation of 64-bit multi-core mobile processors offers unmatched technology for intelligent performance. Its optimized multicore architecture provides better multi-tasking and multi-threaded performance, floating point processing (Intel® AVX) and integrated video features.

With its new generation FPGA and the associated Personality Module, the **IC-INT-VPX3c** is the perfect toolbox to build the most integrated embedded systems.

Moreover, the **IC-INT-VPX3c** is delivered with the IC Boot Loader. This capability to develop optimized UEFI firmwares allows Interface Concept to implement specific functions or services to further improve power-up sequences.

OpenVPX

RoHS ✔
2002 / 95 / EC

Description

The **IC-INT-VPX3c** is a 3U VPX SBC which can act as a System or non-System Controller module in a VPX VITA46 configuration. It is delivered with a Quad Core 3612QE Core i7 Gen3 processor (3517UE/3555LE if power consumption is an heavy constraint of the system).

The **IC-INT-VPX3c** provides the most flexible PCIe Gen2 backplane interface; the lanes from the processor can be used as two x4 ports (P1 A & B) or merged to provide a unique x8 port. The lanes from the QM67 (P1 C) can be used as one fat pipe or four x1 ports for applications claiming for many expansion boards. Note that the **IC-INT-VPX3c** do not use PCIe switch to optimize latency in real-time applications.

The **IC-INT-VPX3c** offers one front GigaEthernet and two GigaEthernet ports on P1 available as 1000BT or 1000BX interfaces.

The **IC-INT-VPX3c** also takes advantage of the media capabilities of the Intel chipset to provide two HDMI interfaces and an HD audio port. A set of serial interfaces (USB and SATA ports) completes this comprehensive range of IO interfaces. For storage, the board also features a SATA SSD module and the option to plug a SATA disk.

Finally, the **IC-INT-VPX3c** implements an Open FPGA interfaced with the CPU (PCIe x4) dedicated to customer applications, for which IC will provide a variety of IPs (additional communications interfaces, GPIOs, video capture...). The selected Kintex-7 FPGAs deliver high signal processing performance, low power consumption and the serial bandwidth claimed by the most demanding embedded applications.

The FPGA is connected directly to the P2 connector (SERDES/GPIOs) and also via a Personality Module to enable a maximum level of integration for hardware specific features.

The **IC-INT-VPX3c** is compliant at least with the following *OpenVPX* Module profiles (VITA 65) :

2F2T   2F2U   3F2U   1D
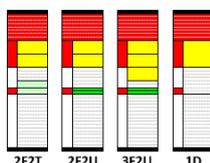
Main features

Processor Unit

► one Intel® Core™ i7 3612QE (other config: 3517UE / 3555LE - consult us)
  • Core speed = 2.1GHz (or 1.7GHz / 2.5GHz)
  • Cache = 6MB (4MB / 4MB)
  • Thermal design power = 35W (17W / 25W)
► DDR3-1333 with ECC (up to 2 * 4 GBytes)
► boot flash memory
► Calendar clock with supercap and/or battery backup
► one thermal monitoring sensor

► a SATA SSD module
► one FPGA (XC7 KX70T / *KX160T on demand*) and a Personality Module.

Communication subsystem

► 3 * GigaEthernet ports   (1000BT ▭ or 1000BX ▬)
► 1 * front RS232 UART
► 3 * USB 2.0 ports (1 front / 2 rear)
► 12 * PCI-Express Gen2 lanes ▭
► up to 4 * rear SATA interfaces
► 2 * HDMI interfaces (1 front / 1 rear)
► 1 * Intel HD Audio interface
► GPIOs (from Personality Module)
► SERDES (from FPGA and Personality Module)

Miscellaneous

► Status Leds
► PIC μ-controller for System Management (per VITA 46.11)

Accessories

► Engineering kit for debug : JTAG/COP, console,...
► 3U Rear Transition Module

The **IC-FEP-VPX3c** is a 3U VPX board compliant with 3U module definitions of the VITA 46.0 standard.

It is available in air-cooled (1") and conduction cooled (0.8") versions compliant with VITA 47 classes.

IC **INTERFACE CONCEPT**

IC-INT-VPX3c

Intel® CoreI7™ Single Board Computer

Boot Loader

Interface Concept Single Board Computers based on Intel CPUs use the new UEFI firrmware technology.
This Boot Loader, **developed and tested by our R&D team**, implements all the initializations and optimized PBITs while ensuring the shortest boot time before launching the UEFI shell or loading the Operating System from storage devices (CD, DVD, HDD, USB…) or network,.

When the final application is running, Runtime services remain in memory allowing thus the user to access UEFI variables for monitoring (e.g. PBIT results) or setup operations.
On request, we can even customize the Boot Loader to keep only what is strictly necessary for customer's applications.

OS support
Interface Concept provides LSP Linux® distributions (IC SDK, others...). For VxWorks® and Windows, please consult us.

Multiware
In oder to empower customers to concentrate their efforts on their most critical tasks, Interface Concept developed a Fabric Management Software implementing optimized services between PCIe domains over non transparent bridges NTB) such as: DMA transfers, Ethernet emulation over PCIe, management of shared memory, messages and semaphores, etc.

Interface features

Front connectors (air cooled versions)

► 1 * GigaEthernet port
► 1 * console port
► 1 * HDMI port
► 1 * USB2 port

P1 connector
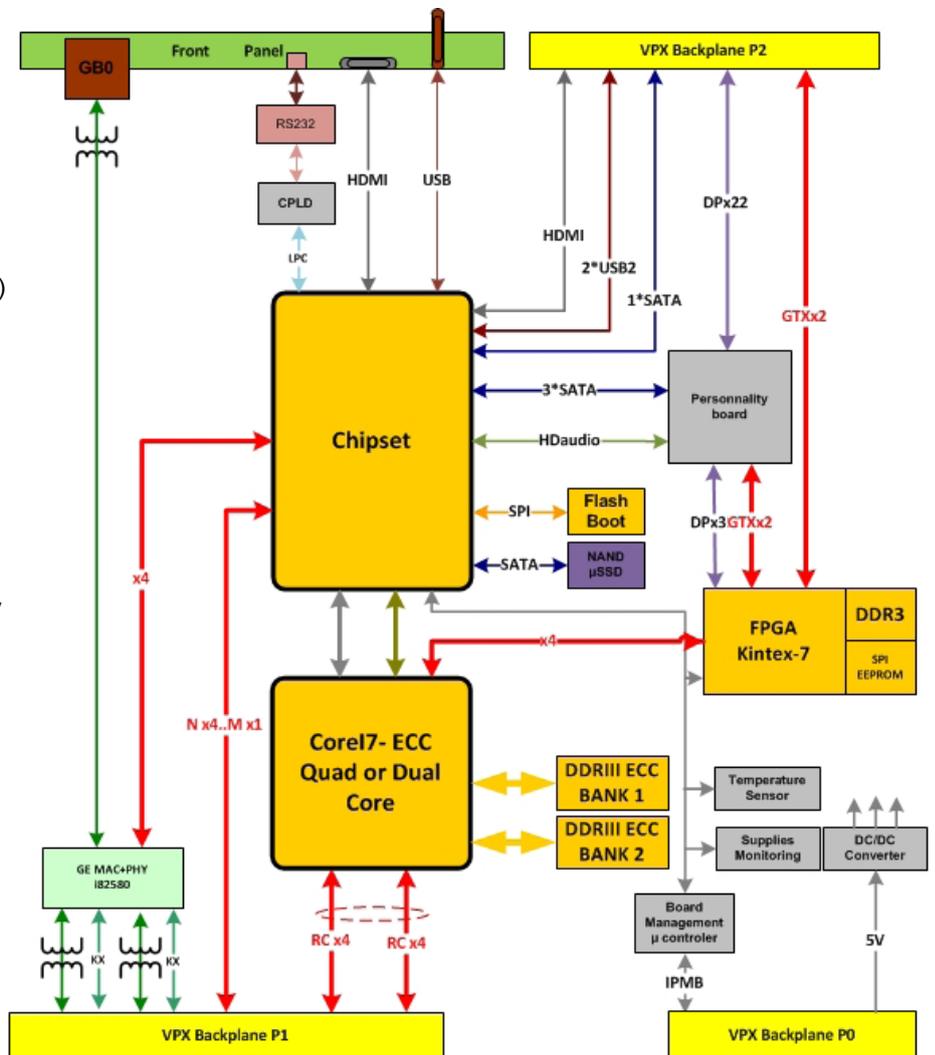
► 8 lanes from the CPU (2*PCIex4 or 1*PCIex8)
► 4 lanes available as one PCIe x4 or four PCIe x1 links (hardware setting) - Port C
► 2 * GigaEthernet ports available either as 2*1000BT interfaces or 2*1000KX (or SGMII) interfaces on P1 (factory setting)

P2 connector

► 2 * USB2 ports
► 1 * SATA ports
► 1 * HDMI port
► GPIOs & SERDES from FPGA & Personality Module
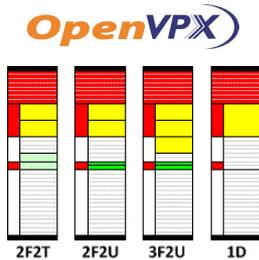
Block Diagram

Environnement Specifications:
Please consult the **IC-INT-VPX3c** page at **www.interfaceconcept.com**.

Ordering Information:
Please contact our sales department : tel. **+33 (0)2 98 57 30 30** - email : **info@interfaceconcept.com**

This document supersedes any earlier documentation relating to the products referred to herein. The information contained in this document is current at the date of publication. It may subsequently be updated or withdrawn without notice.

IC INTERFACE CONCEPT