

The TIC-CMC-VPX3a is a 3U VPX adapter board for PMC or XMC mezzanine modules. Expand the I/O or storage features of your system using a wide range of available modules.

A high performance 3D graphics compute engine can be created when adding Elma's TIC-GRA XMCb graphics module, or designers can create a high-performance and low-power PowerQuicc offload engine with the TIC-PQ3-XMCa. Coupled with an SSD based mezzanine, the TIC-CMC-VPX3a completes the I/O or storage capabilities of a VPX system.

Description

The TIC-CMC-VPX3a is designed to carry one single width XMC board or one single width PMC board.

XMC Configuration:

- 8 lanes are routed from the VPX backplane to the XMC pn5 connector (x1, x2, x4 or x8 PCI-Express configuration supported).
- 64 I/O pins of the Pn6 connector are routed to the VPX P2 connector P2 connector; cabling scheme compliant with VITA 46.9 X8d+X12d+X24s (X38s+X8d+X12d possible on demand)

PMC Configuration :

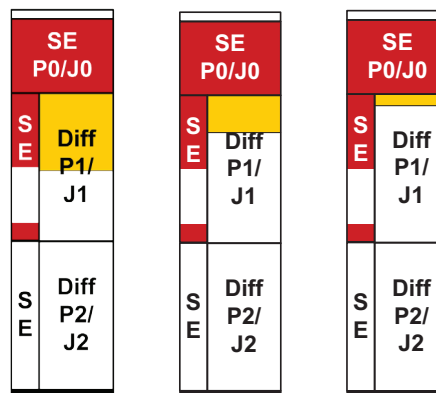
- 4 lanes are routed from the VPX backplane to a PCIe/ PCI bridge supporting:
 - Conventional PCI 32/64 bits 33/66MHz
 - PCI-X 32/64 bits 66/100/133 MHz (3.3V PCI bus signaling)
- 64 I/O pins of the Pn4 connector are routed to the VPX P2 connector (P64s).

Populated with a processor mezzanine board (PMC or XMC), the TIC-CMC-VPX3a can act as a system controller, monitoring power and delivering the VPX 25MHz reference clock. The TIC-CMC-VPX3a is powered from VS3 (5V) which is also used to deliver the VPWR for the XMC module. If 12V is set on VPWR or if more than 3W is required by the mezzanine board on the 3.3V, then versions using the VS1 (+12V) or optional VS2 (+3.3V) are available.

OpenVPX Profile Details

Depending of the features of the PMC or XMC installed, the TIC-CMC-VPX3a will comply with a variety OpenVPX profiles. Examples include:

- SLT3-PAY-1D-14.2.6
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3





VITA



I/O

Main Features

Data plane:

- 8 lanes between VPX P1 (ports A&B) and XMC Jn5, or
- 4 lanes between VPX P1 (ports A) and PCIe/PCI bridge (PMC)

Utility plane:

- Power supplies
- Reset, NVMRO
- Reference clock

Management plane:

- IPMC (VITA46.11)

Rear I/O:

see below

Miscellaneous:

Five LEDs are available on the front panel: Power On, Reset status, Bridge PCIe/PCI link status and Management Controller status (x2).

Front connectors:

- Reset button
- 5 LEDs

P0 connector

- Power supplies
- Reset, NVMRO
- Reference clock

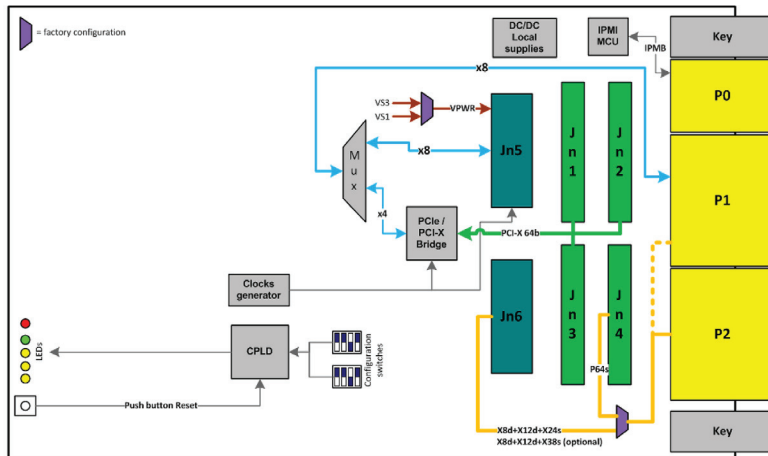
P1 connector

- 8 (or 4) lanes linked to the XMC Pn5 connector (or to the PCIe/PCI bridge)

P2 connector

- 64 I/O pins of the Pn6 connector routed to P2 (compliant with VITA 46.9 X8d+X12d+X24s - X38s+X8d+X12d possible on demand), or 64 I/O of the Pn4 connector routed to tP2 (P64s). (Factory setting)

Block Diagram



Standard Conformance

Emissions

EN55022 Class B

Immunity

CEI 6000-4-2 (ESD), 6000-4-3 (Electric field), 6000-4-4 (Burst), 6000-4-5 (Surge), 6000-4-6.

Security

EN60950

Environmental Specifications

Please visit our website for complete details.

Ordering Information

Model number TIC-CMC-VPX3a

Please contact our sales department at (510) 656-3400 or via email at sales@elma.com for specific model configurations.